CMOS COMPATIBILITY OF A MICROMACHINING PROCESS DEVELOPED FOR SEMICONDUCTOR NEURAL PROBE

S. K. An, S. J. Oh and S. J. Kim

School of Electrical Engineering and Nano Bioelectronics and Systems ERC, Seoul National University, Korea

Abstract – **Neural probes are made on silicon substrate using a micromachining process with low temperature steps only. A deep silicon etch ("Bosch") process was used for the probe shaping. CMOS compatibility of the process was checked and reported in this paper. Test transistor patterns generated using standard CMOS fabrication line were exposed to a post-CMOS probe making process including dielectric deposition, gold metalization and the dry etching step, while changes of test transistor characteristics were monitored. Threshold voltage was found virtually unchanged for both n- and p-type MOS transistors. When excess plasma exposure was done, however, non-trivial shift in p-MOS threshold was observed.**

Keywords – **Neural probes, CMOS compatibility**

I. INTRODUCTION

Silicon-based microelectrode for the neural recording and stimulating have been developed because the silicon microelectrode have many advantages over conventional metal wire bundle[1]. Active circuitry on the silicon microelectrode can be monolithically integrated so that impedance buffering, amplification, and multiplexing can be done[2]. We have previously reported on the process of making a new type of silicon microelectrode[3]. The shank of the microelectrode was made controllable with use of dry etch on the front side and backside. In contrast to the process developed in University of Michigan, our process uses only low temperature steps so it can be applied to completed CMOS chips. The advantage of this approach is that we can use the vendor CMOS services such as MOSIS. This paper reports on the methods and results of the experiments we performed to verify the CMOS compatibility of the probe shaping steps we developed.

II. METHODOLOGY

A. Probe Shaping Process

A needle-like shank of a neural probe was fabricated by isotropic etching of the backside of a silicon wafer after making ridge-like structures on front-side. A deep silicon etch process - called Bosch process - was used. The etch rate was about $2\mu m$/min and the etch selectivity against positive photo-resist was more than 30. When a photo-resist of $5\mu m$ thickness is used, we can easily control the thickness of probe-shank up to $150\mu m$.

B. Test Circuit Design

MOSFET patterns and source-followers were designed in order to specify the CMOS compatibility with the micromachining post-process. We varied the gate lengths of n-type MOSFETs and p-type MOSFETs to be $1.5\mu m$, $2\mu m$, $3\mu m$, and $5\mu m$, with fixed gate widths of $20\mu m$. In addition to the test MOSFET patterns, source-follower that was widely used as a unity gain buffer of typical neurophysiological experiment setup was also integrated. P-type MOSFETs were used because they, with large gate dimensions, are known to have reduced noise levels when used in source-followers[4].

C. Fabrication

The test transistors and circuits were fabricated using a 1.5 μm standard CMOS process service offered by the ISRC(Interuniversity Semiconductor Research Center) of

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Abstract

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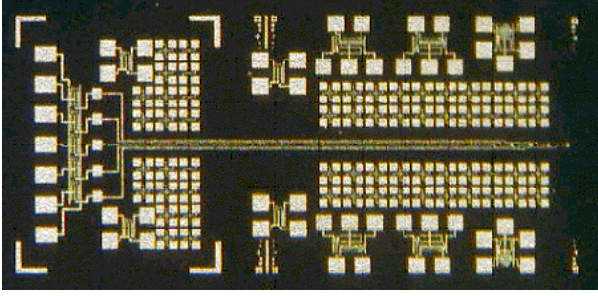| Classification of Abstract	Limitation of Abstract
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Fig.1, Photomicrograph of a completed circuit die. The chip is fabricated using a 1.5μm CMOS process with a die size of 3mm x 6mm.
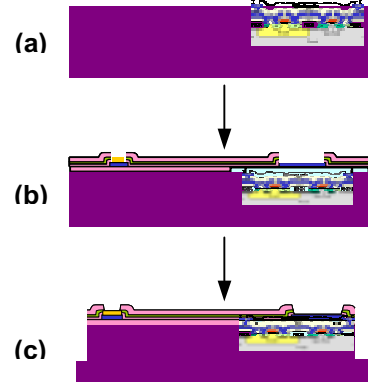

Fig.2, Process flow of the probe-shaping micromachining process. (a) standard CMOS process, (b) Dielectric deposition, Au metalization and site opening, (c) Deep silicon etch process.

the SNU(Seoul National University). This process is a double metal, single poly process with a gate oxide thickness of 250Å. After the CMOS process, the micromachining process discussed above was performed to achieve the structure of the neural probe. Figure 2 shows the process flow. First, a triple dielectric layer consisting of PECVD silicon dioxide(200nm), silicon nitride(200nm), and silicon dioxide(800nm) was deposited on the wafer completed with the CMOS process. The recording sites were then opened by plasma etch and inlaid with gold. Bonding pads were also opened as shown in figure 2(b). The front side of a wafer was then etched to make the ridge-like structures as shown in figure 2(c). This Bosch process was done at 9W power for 45minutes. Finally the backside of the wafer was etched out using isotropic etching and the process was completed.

D. Measurement

In order to verify the CMOS compatibility of the post-CMOS micromachining process, the threshold voltages of test MOS patterns and the DC characteristics of source-followers were measured at the following three phases: 1) after the standard CMOS process, 2) after the site opening and gold metalization, and 3) after the deep silicon etching. A probe station and a semiconductor parameter analyzer (4155A, Hewlett Packard) were used in circuit tests.

III. RESULTS

Figure 3 shows the microphotography of a completed neural probe that contain on-chip source-followers and test MOSFET patterns. The shank-thickness was 60μm. This should well penetrate pia and dura maters of some animals without breakage [5]. The fabricated structure using Bosch process is proven as flexible as the one we earlier made with LTO/dry etch process [3], in terms of controlling the shank thickness.

Figure 4(a) and (b) show the measured threshold voltages of test transistors. Both threshold voltages of n-type and p-type transistors remain virtually unchanged after the Au metalization and deep dry etch. However, when additional plasma dry etch process was performed on the backside of the wafer at 200W power for 240mins to remove the excess silicon by dry etch, a shift in threshold was observed especially in p-type MOSFETs. Nevertheless, the DC characteristics of source-followers were not seen significantly altered by this threshold shift as shown in Figure 4 (c).

IV. DISCUSSION AND CONCLUSION

We have developed a neural probe-shaping process based on a deep silicon etch. This process is effective in controlling the shank thickness as in the other process we previously reported using LTO/dry etch. In order to verify

the CMOS compatibility of the said process, we designed MOS patterns and a source-follower, and tracked their characteristics at three phases of the process. We could verify the CMOS compatibility of the process and proved that the low power Bosch etch process did not cause significant plasma damage that causes threshold changes. However, when a plasma etch process at higher power and for longer duration was added, some shifts in thresholds (a shift of a few tenths of a volt) occurred in the case of p-type MOS. The reason why it affected p-type MOS but not the n-type one, requires further investigation. Furthermore, such high power, MOS-damaging plasma etch process for the backside would not be required if the backside etch is done employing one of the widely used wet chemical etching techniques, such as EDP and KOH etching.
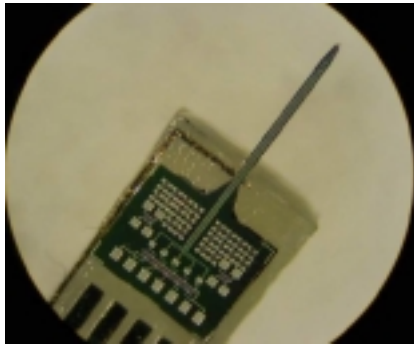

Fig.3, Photograph of a silicon microelectrode with on-chip test MOSFET patterns and source-followers. The overall length of the probe is 6mm.

(a)
Gate Length vs Threshold Voltage (PMOS)

(b)
Gate Length vs Threshold Voltage (NMOS)

(c)
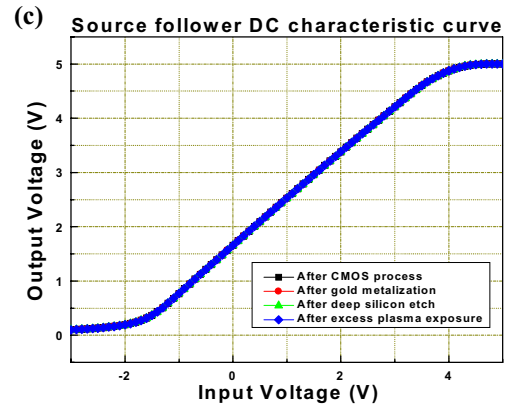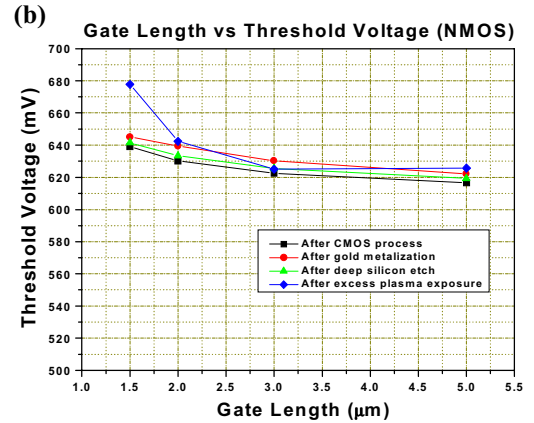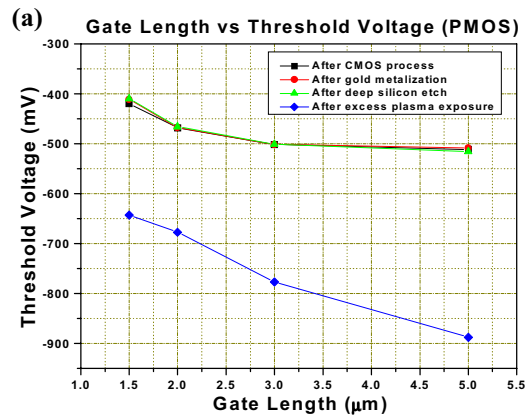**Source follower DC characteristic curve**

Fig.4, The changes of DC characteristics during the probe-shaping micromachining process of (a) PMOSFETs, (b) NMOSFETs, and (c) source followers.

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